

Non-contact addressing of toroid-shaped vertical giant-magnetoresistive random access memory elements

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Researchers will present experimental switching data demonstrating giant-magnetoresistive (GMR) memory bits fabricated with non-contact address lines designed to facilitate two-dimensional selection and optimize density. Originally devised and developed by Dr. G.A. Prinz, et al, of the Naval Research Laboratory and Dr. J. Zhu, of Carnegie Mellon University, vertical GMR memory¹ is a high-density form of non-volatile magnetoresistive random access memory (MRAM) that scales to an estimated 400 Gbits/in.² and, unlike other MRAM technology, does not require a transistor per cell. Simulations performed by Dr. Zhu indicate that for a baseline magnetic stack design a read function requires ten milliamps of bit line current with five milliamps of address line current, while a write requires fifteen milliamps of bit line current with ten milliamps of address current. Initial experimental data on the switching behavior of sixty-four-bit strings of magnetic cells shows that corresponding read switches are occurring at seven milliamps of bit line current with four milliamps of address current and write switches are occurring at fifteen milliamps of bit line current with eight milliamps of address current. MRAM, in general, has the speed and density to replace current semiconductor memories and, at the densities projected, vertical MRAM has the potential to compete with mechanical hard disks, especially in applications where systems are difficult to access.

¹Zhu, J., Zheng, Y., and Prinz, G.A. "Ultrahigh density vertical magnetoresistive random access memory (invited)." Journal of Applied Physics. Vol. 87, Num. 9. 1 May 2000.